

**DUAL-BIT DOUBLE-POLYSILICON SOURCE-SIDE INJECTION  
FLASH EEPROM CELL**

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**ABSTRACT OF THE INVENTION**

10 A four-terminal dual-bit double-polysilicon  
source-side injection flash EEPROM cell, capable of  
storing two bits of information includes a right  
junction (which can serve as a cell drain or a source),  
a left junction (which can serve as a cell source or  
15 drain), a select-gate, and two floating gates. The two  
floating gates are insulated from the select-gate by an  
inter-gate dielectric. The inter-gate dielectric has a  
"weak region" so that during erase-mode electrons can  
tunnel from the floating gate to the select-gate. The  
20 two bits in the cell are to be separately read or  
programmed, but are to be erased simultaneously.  
Programming of each bit is achieved through hot-carrier  
injection, while simultaneous erase of the two bits is  
achieved through electron-tunneling.